Field Emission from Silicon Tips Embedded in a Dielectric Matrix

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***Abstract*—In this work, we present FEAs based on silicon field emitter tips on top of silicon nanowires with four different device structures: (a) buried tips, (b) buried tips with graphene, (c) released tips, and (d) released tips with graphene. Measured device parameters are used to characterize the performance of the devices. In general, we obtain low turn-on voltages when b_{FN} is low. Additional studies of current variations are required.**

Keywords*—*FEA, field emitter tip, dielectric matrix, graphene, silicon

I. Introduction

Field emitter arrays (FEAs) are a class of cold cathodes with promising potential in a variety of applications requiring high current density electron sources. However, FEAs are yet to achieve widespread usage because of fundamental challenges that limit their lifetime in systems. These challenges include (a) tip burn-out due to Joule heating and thermal run-away, (b) dielectric breakdown of the gate electrode stand-off insulator, and (c) tip erosion by ions streaming back to the tip due to ionization of residual or adsorbed gas molecules. In addition, field emission from conducting surfaces requires high fields and pristine surfaces. These surfaces are vulnerable to adsorption-desorption processes by residual gas molecules leading to emission current fluctuations. Moreover, electron transport through insulators often leads to impact ionization and dielectric breakdown. This work explores electron emission from field emitter tips that are embedded in a dielectric matrix, specifically silicon dioxide, as a potential approach to address lifetime problems in classical field emitters.

II. Device Structure and Fabrication

The devices presented in this work are arrays of silicon field emitter tips that are individually regulated by silicon nanowires [1]. The silicon nanowires have diameters between 100-200 nm and heights of 10 µm resulting in an aspect ratio of 50-100:1. The emitter tips have radii of 5 nm with a log-normal distribution (σ = 1.2 nm) and a density of 10^8 tips/cm^2. Further, the silicon nanowires function as current limiters which improve lifetime by preventing premature tip burn-out due to Joule heating, thermal runaway, and cathodic arcs. Chemical mechanical polishing (CMP) was used to form the self-aligned gates. We explored four device structures with the following properties: (A) Si tips embedded in 50 nm of SiO_2, (B) Si tips embedded in SiO_2 & having a graphene layer on the gate, (C) Si tips released, and (D) Si tips released & having a graphene layer on the gate. Using the technique reported in [2], a single layer of graphene was deposited on a copper substrate and transferred on top of the polysilicon gates using PMMA. The graphene layer creates an equipotential surface above the tips. A diagram of two of the final structures [(B) & (D)] with a single layer of graphene on the gate is shown in Fig. 1.

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III. Device Characterization

The anode current and gate current were measured for different size arrays in a UHV chamber with the anode biased at 1100V with 1 cm separation from the FEA. Fig. 2 presents the anode current data collected for 32x32 arrays for each device configuration. From the data, we obtained the turn-on voltage, $V_{GE,on}$, of the array and extracted the slope of the Fowler-Nordheim plot, b_{FN}. In order to gauge the performance and stability of the device, we calculated the mean anode current per tip at a fixed voltage and the range about the mean, ΔI_A, given as a percentage of the mean current. Table 1 gives a summary of important parameters for four different 32x32 FEAs fabricated using each of the four device structures.

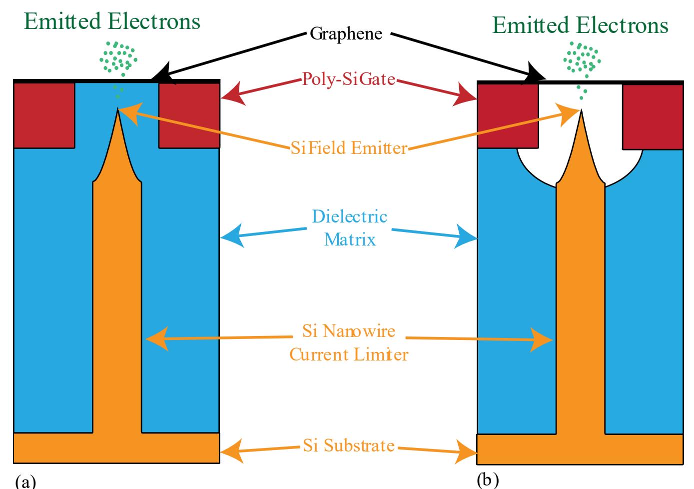

Fig. 1. Cross-section of a Si FEA with a single layer of graphene on the gate electrode showing (a) tip embedded in SiO_2 and (b) tip released.

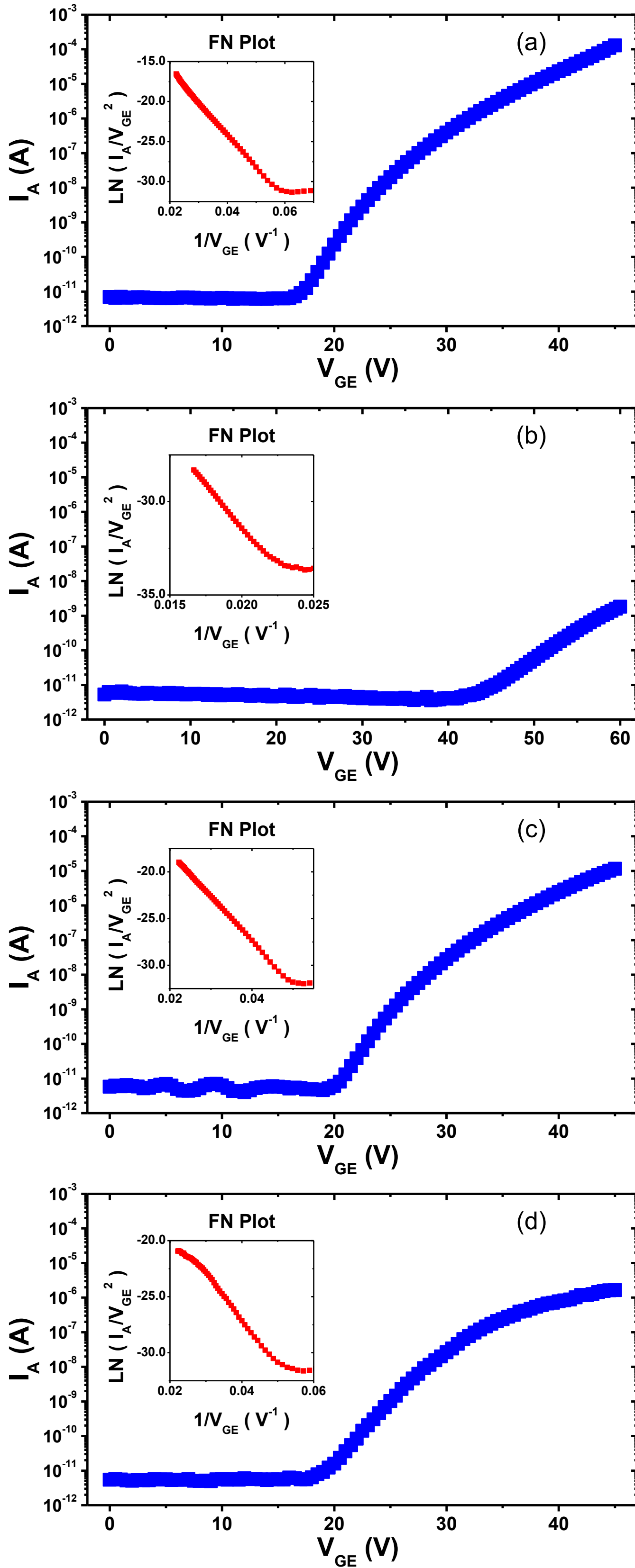

Fig. 2. I-V characteristics of a 32x32 FEA with device structure (a) buried tips (b) buried tips with graphene (c) released tips (d) released tips with graphene

TABLE I. SUMMARY OF DEVICE CHARACTERIZATION DATA

32x32 FEA	Device Structures			
	(A) Buried Tips	*(B)* Buried w/ Graphene	*(C)* Released Tips	*(D)* Released w/ Graphene
b_{FN} (V)	421	940	475	410
$V_{GE,on}$ (V)	17	44	20	18
I_A/tip (nA) @V_{GE}=45V	127	1.77 pA @60V	11.3	1.68
ΔI_A	38.6%	64.8%	8.13%	40.0%

IV. DISCUSSION

Comparing device structures (a), (c), and (d), we observe that they have similar characteristics as evidenced by b_{FN} and $V_{GE,on}$. However, the FEA with buried tips and single layer graphene on top showed considerably different performance from the other device structures; the device had a higher b_{FN} of 940, and the turn-on voltage was higher by ~25V. Interestingly, the anode and gate current have nearly identical b_{FN}. As a result, we suggest that the tunneling mechanism in this device structure is the same for both anode and gate current, and the graphene behaves as a one-directional transmission screen for electrons. Because the gate and anode current are parallel with nearly identical b_{FN}, we can treat this device similarly to a BJT and analyze the electron transmission through the graphene by calculating the common-gate current gain (I_A/I_E). We obtain an electron transmission efficiency of 4.3% which is reasonable for electrons with energies of a few tens of eV [3]. In addition, the range about the mean anode current provides an approximation to the emission current fluctuation. For FEAs with either or both buried tips and graphene, we see higher variation in current due to electron transport effects through the SiO_2 and graphene. The FEA with the released tips had the smallest range due to the absence of these effects. Finally, we speculate that the SiO_2 or graphene layer could protect the emitter tip from back-bombarding ions and prevent tip erosion, and hence potentially allow FEAs to operate in a poor vacuum. However, additional studies are required to understand and mitigate the variations in current.

V. SUMMARY

In this work, we reported Si FEAs fabricated with four different tip structures that are potentially suitable for high current density applications. Several parameters were extracted from measured data in order to determine the performance of the devices. Additional studies of current variations and lifetime are required.

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